

The opinion in support of the decision being entered today
is *not* binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LI FUNG CHANG, and MARK D. HAHM

Appeal 2007-1653
Application 10/791,945¹
Technology Center 2600

Decided: September 28, 2007

Before: ANITA PELLMAN GROSS, ALLEN R. MACDONALD, and
MARC S. HOFF, *Administrative Patent Judges.*

HOFF, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of
claims 1-31. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

¹ Application filed March 3, 2004. The real party in interest is Broadcom Corporation.

Appellants' invention relates to improved processing of data communications received by a wireless terminal. Specifically, Appellants disclose a method and system for implementing Incremental Redundancy (IR) operations in a wireless receiver, including a system processor operable to receive the soft decision bits of a data block, to configure the plurality of IR processing module registers, initiate operation of the IR processing module of the wireless receiver, access the plurality of IR processing module registers, and perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block (Specification 5).

Claim 1 is exemplary:

1. A method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising:

receiving an analog signal corresponding to a data block;

sampling the analog signal to produce samples;

equalizing the samples to produce soft decision bits of the data block;

configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers;

initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and

accessing, by the IR processing module, the plurality of IR processing module registers; and

performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Parolari	US 2004/0081248 A1	Apr. 29, 2004
Ramesh	US 6,909,758 B2	Jun. 21, 2005

Claims 1-7, 9-11, 13-22, 24-26, and 28-31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Parolari.²

Claims 8, 12, 23, and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Parolari in view of Ramesh.

Claims 1, 12, 16, 27, and 31 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 6, 7, 14, 27, 28, and 34 of copending Application No. 10/731,803.³

Appellants contend that Parolari does not teach the claim limitations of “configuring,” “initiating,” “accessing,” and performing,” as recited in full *supra*. The Examiner contends that the various general teachings regarding incremental redundancy, found in diverse sections of Parolari, are sufficient to meet these limitations.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants could have made but chose not to

² The rejection of claims 1, 3-5, 7, 11, 16, 18-20, 22, 26, and 29 under 35 U.S.C. § 102(b) as being anticipated by Pukkila has been withdrawn by the Examiner.

³ The Brief and Answer refer to a provisional double patenting rejection. However, with the issuance of Application No. 10/731,803 on January 16, 2007 as U.S. Patent No. 7,164,732, this rejection is no longer provisional.

make in the Briefs have not been considered and are deemed to be waived.
See 37 C.F.R. § 41.37(c)(1)(vii) (2004).⁴

ISSUE

The principal issue in the appeal before us is whether the Examiner erred in holding that Parolari teaches the steps of “configuring,” “initiating,” “accessing,” and “performing,” as recited in claims 1 and 16.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. Appellants invented a method and system for improved performance in Enhanced Data rates for GSM Evolution (EDGE) Incremental Redundancy (IR) operations in a wireless receiver (Specification 4-5).
2. Appellants’ system includes a system processor, a plurality of IR processing module registers, and an IR processing module (Specification 5).
3. The system processor is operable to receive the soft decision bits of a data block, to configure the plurality of IR processing module registers, initiate operation of the IR processing module of the wireless

⁴ Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young*, 927 F.2d 588, 590, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). *See also* 37 C.F.R. § 41.37(c)(1)(vii).

receiver, access the plurality of IR processing module registers, and perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block (Specification 5).

Parolari

4. Parolari teaches an improved method of link adaptation in enhanced cellular communication systems to discriminate between lower or higher variable RF channels with or without incremental redundancy (para. [0002]).

5. Appellants concede that Parolari meets the claimed steps of receiving an analog signal corresponding to a data block, sampling the analog signal to produce samples, and equalizing the samples to produce soft decision bits of the data block (Br. 17).

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR Int'l. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007) (citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329,

1336 (Fed. Cir. 2006)). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellant. *Piasecki*, 745 F.2d at 1472, 223 USPQ at 788. Thus, the Examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the Examiner's conclusion.

Non-statutory, or "obviousness-type," double patenting is a judicially created doctrine adopted to prevent claims in separate applications or patents that do not recite the "same" invention, but nonetheless claim inventions so alike that granting both exclusive rights would effectively extend the life of patent protection. *Gerber Garment Tech., Inc. v. Lectra Sys., Inc.*, 916 F.2d 683, 686, 16 USPQ2d 1436 (Fed. Cir. 1990) (citing *In re Thorington*, 418 F.2d 528, 534, 163 USPQ 644, 648 (CCPA 1969)).

ANALYSIS

Appellants argue that Parolari does not anticipate the claims because the sections of Parolari cited by the Examiner teach some of the elements of the claims (FF 5), and describe generally some aspects of an incremental redundancy (IR) process, but do not teach or suggest, as recited in claim 1:

- configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers;
- initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and
- accessing, by the IR processing module, the plurality of IR processing module registers; and
- performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

Appellants point out that Parolari “describes generally how a control processor oversees/controls IR processing and how RLC blocks may be stored in an IR buffer for retransmission, not storage of received punctured data blocks” (Br. 17) but does not disclose “any other structure that performs IR processing of received punctured data” (Br. 17).

We agree with Appellants. Paragraph [0112] of Parolari, cited by the Examiner as teaching the four steps *supra*, contains general discussion of incremental redundancy, and mentions soft decision bits, but fails to teach or suggest the specific operations claimed by Appellants. In response to Appellants’ Brief filed October 16, 2006, the Examiner attempted to buttress his holding of anticipation by referring the reader to paragraphs [0051], [0061], [0074] and [0117] of Parolari as well. While we agree that these sections do contain general discussion of incremental redundancy (IR) techniques, none teaches any of the specific steps of configuring, initiating, accessing or performing which Appellants contest. We have reviewed Parolari in full and can find no teaching of these specific limitations. Similar limitations are also present in independent claim 16. Accordingly, we reverse the rejection of claims 1-7, 9-11, 13-22, 24-26, and 28-31 under 35 U.S.C. § 102.

Claims 8, 12, 23 and 27, each dependent from either claim 1 or claim 16, stand rejected as obvious over the combination of Parolari and Ramesh. As noted *supra*, Parolari does not meet the limitations of parent claims 1 and 16. Ramesh fails to teach the elements not present in Parolari. We therefore reverse the rejection of claims 8, 12, 23, and 27, under 35 U.S.C. § 103.

Appellants explicitly stated that they did not address the double patenting rejection present in the application (Br. 5). We therefore affirm the Examiner's obviousness-type double patenting rejection of claims 1, 12, 16, 27, and 31.⁵

CONCLUSION OF LAW

We conclude that Appellants have not shown that the Examiner erred in rejecting claims 1, 12, 16, 27, and 31 on double patenting grounds. Claims 1, 12, 16, 27, and 31 are not patentable. We conclude that Appellants have shown the Examiner erred in rejecting claims 1-7, 9-11, 13-22, 24-26 and 28-31 under 35 U.S.C. § 102, and claims 8, 12, 23 and 27 under 35 U.S.C. § 103. On the record before us, claims 1-31 have not been shown to be unpatentable with regard to 35 U.S.C. §§ 102 and 103.

DECISION

The Examiner's rejection of claims 1-7, 9-11, 13-22, 24-26 and 28-31 under 35 U.S.C. § 102, and of claims 8, 12, 23 and 27 under 35 U.S.C. § 103 is reversed. The Examiner's double patenting rejection of claims 1, 12, 16, 27, and 31 is affirmed. Because we have affirmed at least one rejection of some of the claims, we affirm-in-part.

⁵ As noted *supra*, the conflicting application has subsequently issued as U.S. Patent No. 7,164,732; therefore, the double patenting rejection of record is no longer provisional.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a). See 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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